

**REMARKS**

Favorable consideration and allowance of the claims of the present application are respectfully requested.

In the present Official Action, Claims 1-30 which are present in the above-captioned application have been subjected to a restriction under 35 U.S.C. §121 as follows:

- I.       Claims 1-20 and 28-30, drawn to a method of correcting a logic failure in an IC by using an FPGA, classified in Class 714, subclass 3;
- II.      Claim 21, drawn to a method of evaluating simulated errors by injection, classified in Class 716, subclass 4; and
- III.     Claims 22-27, drawn to an IC and method with the IC including an ICE, and using an FPGA to correct logic errors, classified in class 703, subclass 28.

As indicated, and in order to be fully responsive to the restriction requirement imposed in the present Official Action, applicants provisionally elect, without traverse, to prosecute the subject matter of Group I, i.e., Claims 1-20 and 28-30, and reserve the right to file one or more divisional applications directed to the non-elected subject matter in this application, i.e., Claims 21-27.

Wherefore, consideration and allowance of the claims of the present application are respectfully requested.

Respectfully submitted,



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